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VHDL Implementation of All Digital OFDM Modulator and Demodulator for Wireless Broadband Applications (FPGA)

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Abstract: The new mobile technologies trying to give broadband over wireless channel allowing the user to have bandwidth connectivity even inside moving vehicle. The metropolitan broadband wireless networks require a non-line-of-sight (NLOS) capability, and the scheme Orthogonal Frequency Division Multiplex (OFDM) becomes essential to overcome the effects of multipath fading. Orthogonal Frequency Division Multiplexing (OFDM) has become very popular, allowing high speed wireless communications. OFDM could be considered either a modulation or multiplexing technique and its hierarchy corresponds to the physical and medium access layer. A basic OFDM modulator system consists of a QPSK modulator, a serial to parallel, and an IFFT module. The iterative nature of the IFFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. The VHDL implementation allows the design to be extended for either FPGA or ASIC implementation, which suits more for the Software Defined Radio (SDR) design methodology. In this project the OFDM modulator and demodulator will be implemented with full digital techniques. VHDL will be used for RTL description and FPGA synthesis tools will be used for performance analysis of the proposed core. The major blocks are Interleaving/Mapping circuit, 8 point IFFT, 8 point FFT, and arithmetic blocks. Modelsim Xilinx Edition will be used for functional simulation and verification of results. Xilinx ISE will be used for synthesis. The Xilinx's chip scope tools will be used for verifying the results onSpartan3E FPGA.

Keywords: OFDM; IFFT; FFT; FPGA; VLSI.

I. INTRODUCTION

The Telecommunications industry faces the problem of providing telephone services to rural areas, where the customer base is small, but the cost of installing a wired phone network is very high. One method of reducing the high infrastructure cost of a wired system is to use a fixed wireless radio network. The problem with this is that for rural and urban areas, large cell sizes are required to obtain sufficient coverage. This result in problems caused by large signal path loss and long delay times in multipath signal propagation. Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream. OFDM is similar to FDMA in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels, which are then allocated to users. However, OFDM uses the spectrum much more efficiently by spacing the channels much closer together. This is achieved by making all the carriers orthogonal to one another, preventing interference between the closely spaced carriers.

Rest of the paper is organized as follows Section II describes the FPGA VLSI design, Section III Describe OFDM architecture, Section IV describes Implementation and results section V describes results, and Section VI Describes conclusion, VII Describes References the paper.

II. FPGA AND VLSI DESIGN

Recent strides in programmable logic density, speed and hardware description languages (HDL's) have empowered the engineer with the ability to implement digital signal processing (DSP) functionality within programmable logic devices (PLDs or FPGAs). In this chapter the VLSI design methods on FPGAs using VHDL are discussed. The FPGA architectures basics are also discussed. The following section presents fundamentals of VHDL and synthesis issues related to it.

VHDL is a high level description language for system and circuit design. The language supports various levels of abstraction. In contrast to regular net list formats that supports only structural description and a Boolean entry system that supports only dataflow behavior, VHDL supports a wide range of description styles. These include structural descriptions, dataflow descriptions and behavioral descriptions. VHDL is fully simulatable, but not fully synthesizable. There are several VHDL constructs that do not have valid representation in a digital circuit. The first type of user-programmable chip that could implement logic circuits was the Programmable Read-Only Memory (PROM) The first device developed later specifically for implementing logic circuits was the Field-Programmable Logic Array (FPLA), or simply PLA for short. A PLA consists of two levels of logic gates: a programmable "wired" AND-plane followed by a programmable "wired" OR-plane. Many commercial FPD

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products exist on the market today with this basic structure, and are collectively referred to as Complex PLDs (CPLDs).

CPLDs were pioneered by Altera, first in their family of chips called Classic EPLDs , and then in three additional series, called MAX 5000, MAX 7000 and MAX 9000 (MAX-Multiple Array Matrix). Because of a rapidly growing market for large FPDs, other manufacturers developed devices in the CPLD category and there are now many choices available. CPLDs provide logic capacity up to the equivalent of about 50 typical SPLD devices, but it is somewhat difficult to extend these architectures to higher densities. To build FPDs with very high logic capacity, a different approach is needed. Xilinx introduced the first FPGA family, called the XC2000 series, in about 1985 and now offers three more generations: XC3000, XC4000, and XC5000. Although the XC3000 devices are still widely used, we will focus on more popular XC4000 family. We note that XC5000 is similar to XC4000, but has been engineered to offer similar features at a more attractive price, with some penalty in speed. We should also note that Xilinx has recently introduced an FPGA family based on anti-fuses, called the XC8100, but since it is not in the scope of the project Top down Design Flow with Precision RTL Synthesis is shown in Fig. 1.

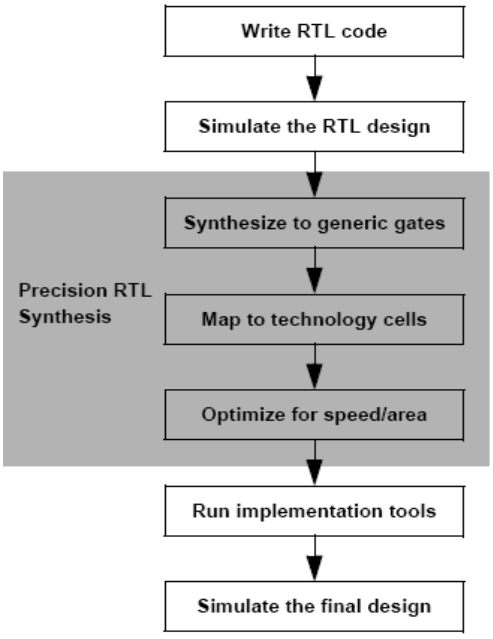


Figure1: Process to VLSI Implementation (FPGA, ASIC)

OFDM Benefits: Need for OFDM and benefits is it is a broad band multicarrier modulation method that offers superior performance and benefits over older more traditional single carrier modulation methods because it is a difficult with today's high speed data transmission for UHF and microwave spectrum. OFDM is accomplished with DSP we can program the IFFT and FFT math functions on any fast pc with today's superfast chips even complex math routines like FFT are relatively easy to implement.

1) Spectral efficiency
2) Maximum data rates for a given BER and noise level

III. OFDM ARCHITECTURE

A.OFDM Modulator Blocks

1) Clock distributor: clock distributor is distribute the clock equally for our application requirements we can use 1MHz clock for my modulator and demodulator circuit the entire project run in 1MHz clock only. Where the input is clock and output get the two signals that are div/2, div/16. Two signals applicable for serial to parallel convertor and IFFT. Remaining blocks can operate in master clock.

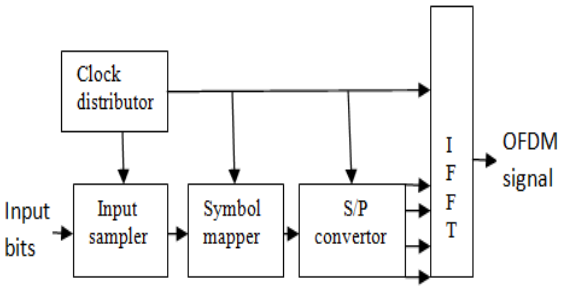


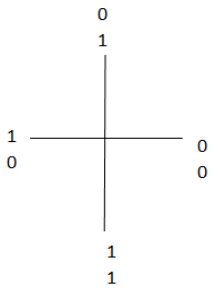
Figure2: OFDM Modulator

2) Input sampler: input signal is sequence of data when the given input is'0' and '1'to continuously to get out at two bits data 00,01,10,11 rapidley. where the input sampler data pass into symbol mapper.

3) Symbol mapper: output of the input sampler is connected to symbol mapper input. Where the two inputs of data to receiving symbol mapper where it is converted into real and imaginary parts. Consolation is bit stream as input and to convert into symbols. Why we are dividing real and imaginary parts where the long transmission bulk amount of data will occur in additional unwanted bits and calculations is more difficult for the higher order modulation schemes.

Dibit	phase
00	0
01	90
10	180
11	270

Dibit (2 bits)



Consolation

4) Serial to parallel convertor (SIPO): OFDM system each channel is can be broken into various sub carriers; the use of sub carriers makes optimal use of the frequency spectrum but also requires additional processing by the transmitter and receiver. The additional processing is necessary to convert a serial bit stream into parallel bit stream to be divided among the individual carriers. Once

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the bit stream has been divided among the individual sub carriers each sub carrier is modulated as if it was an individual channel before all channels are combined back together transmitted as a whole. The receiver performs the receiver process to divide the incoming signal into appropriate sub carrier and then demodulating these individually before re constructing the original bit stream.

5) IFFT: It is converted into frequency division into time division everyone knows that but why we using in IFFT in receiver only and sometimes input signal in time do main nature so why we can convert into time domain again? IFFT comes handy in implementing the conversion process and we can eliminate the individual sinusoidal multipliers required in the transmitter and receiver. Use of IFFT in the transmitter eliminates the need for separate sinusoidal converts always remember that IFFT and FFT in the transmitter are interchangeable as long as their dual are used in receiver.

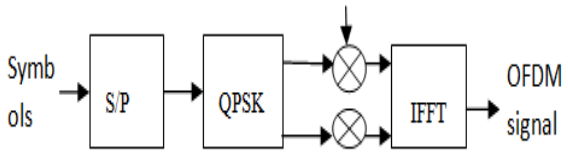

Figure 5: IFFT output using S/P

Where the output of the serial to parallel convertor is connected into IFFT where the real and imaginary parts of the data is butterfly and twiddle factor output are consulates then equal to the OFDM signal and sum of the mathematical calculations to perform and it is equal to the IFFT.

B) OFDM Demodulator:

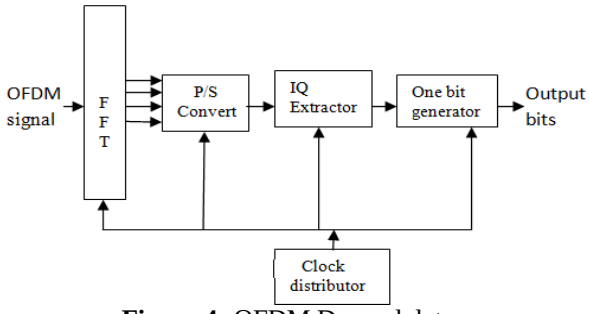

Figure 4: OFDM De modulator

1) FFT: convert time domain into frequency domain where the receiving of the IFFT output is connected to FFT.Each contain one signal made up of n complex points each of this complex points are composed of two points real and imaginary.FFT operates by decomposing on N point time domain signal into N time domain signal each composed of a signal points. Second step is calculate the N frequency spectra corresponding to these N time domain signals the N spectra as synthesized into a single frequency spectrum. FFT bit reversal sorting the FFT time domain de composition can be implemented by sorting the samples according to bit reversal order. By using IFFT/FFT operate in OFDM-LTE channel is divided into many narrower channels with lower rates and hence longer symbol duration to reduce problems with multipath reflections

2) Parallel to serial convertor (PISO): what we have received in the FFT output signal is connected to parallel to serial convertor input signal. Reverse process of the serial to parallel converter, where the parallel to serial convertor have one shift register inside where the parallel data have received in input it will move to shift register and taken bit by bit data it is equal to the input signal of the serial to parallel converter; this bock is used to convert the data obtained from the FFT into serial data and is fed as input to the symbol demapper.

3) Symbol Demapper: input is fed from the parallel to serial convertor, from received real and imaginary parts based on fixed threshold values. Each adjacent channel difference by one bit, it is equal to the half of the amplitude of the input value; totally this blocks works on QPSK modulation technique. Real and imaginary values will converted into a two bit sequence.

4) One Bit Generator: input is fed from symbol de mapper this block takes two bits data from IQ extractor and generates output bit sequence, what we given in the input bit sequence 128 bits of data will present in the one bit generator.

IV. IMPLIMENTATION AND RESULTS

The work presented in this paper aimed in demonstrating the capability of a straight forward translation of wireless communication system into a pure VHDL implementation on reconfigurable platform. The work has accomplished the task of designing modulator and demodulator. Results are driven for the transmitter block using Xilinx, Codes are completely in VHDL.All blocks designed in individually and combined one top module for modulator and demodulator and verify the mapping functionality and routing in Xilinx ISE.

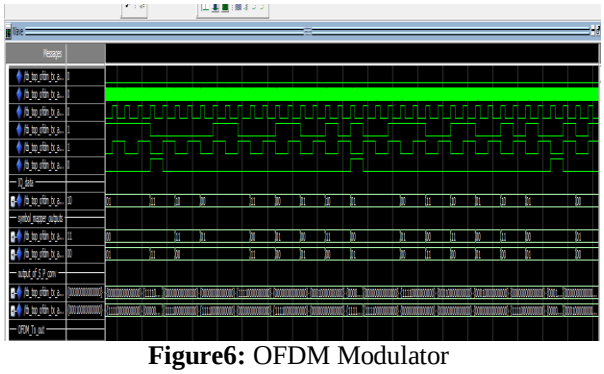

Figure6: OFDM Modulator

In this modulator included in clock distributor operate in 1MHz clock operates and then using input samplers to pass continues bit sequences and convert to two bit data.

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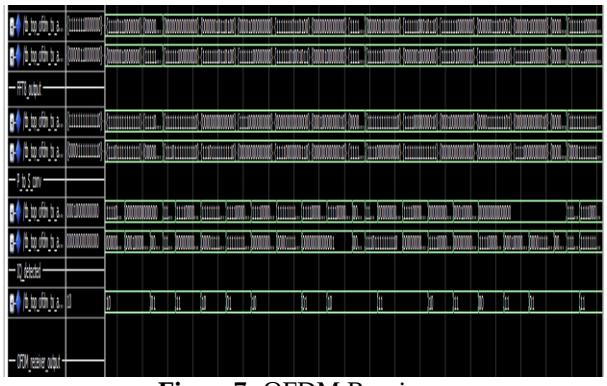

Figure7: OFDM Receiver

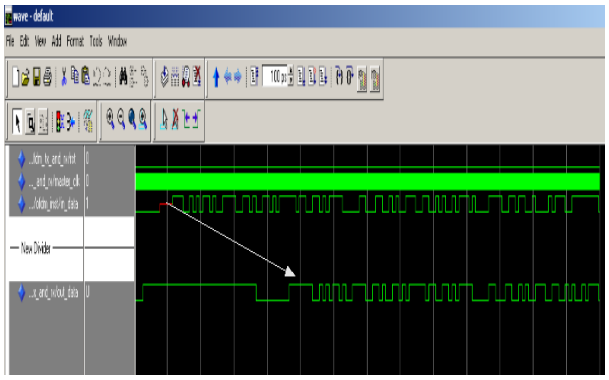

Figure 8: OFDM Transmitter and Receiver

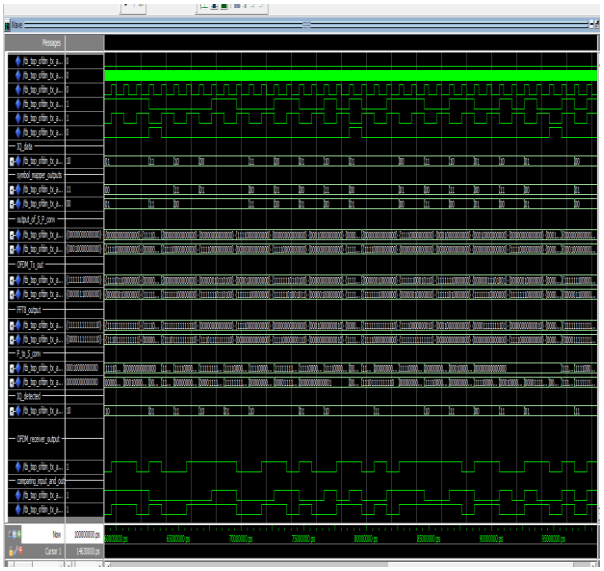

Figure9: OFDM Modulator Demodulator Top Block

In this RTL schematic represents OFDM modulator and demodulator outputs. Last two signals are modulator input and demodulator output presentation the signals same with initial delay because of transmitted 140 bits of data and my data is 128 bits remaining 12 bits initial zeros. Why using 12 initial zeros whenever the any unwanted and over flow bits occur in the my bit sequence no effected on given input signal, seeing the RTL is in Modelsim and Xilinx also code dump in to Spartan 3E FPGA kit and observed results in chip scope analyzer tool in command window. The result of the chip scope analyzer tool is

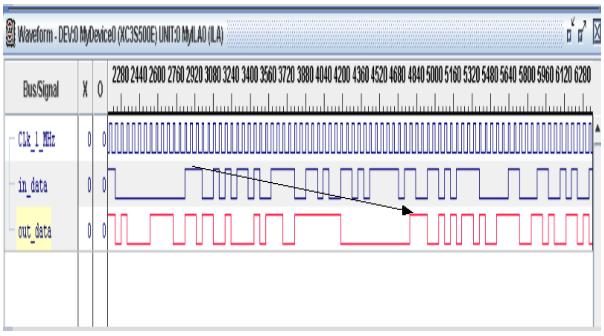

Figure 10: chip scope output

All code simulates first and after convert to UCF file then dumps into Spartan 3E FPGA and observed results in command window.

Table I resource utilization summary

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	443	9,312	4%
Number of 4 input LUTs	7,923	9,312	85%
Number of occupied Slices	5,406	4,656	116%
Number of Slices containing only related logic	5,406	5,406	100%
Number of Slices containing unrelated logic	0	5,406	0%
Total Number of 4 input LUTs	9,679	9,312	103%
Number used as logic	7,867		
Number used as a route-thru	1,756		
Number used as Shift registers	56		
Number of bonded IOBs	3	232	1%
Number of RAMB16s	1	20	5%
Number of BUFGMUXs	3	24	12%
Number of BSCANs	1	1	100%
Number of MULT 18X 18SIOs	16	20	80%
Number of RPM macros	12		
Average Fanout of Non-Clock Nets	2.34		

Table II Device utilization summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4421	4656	94%
Number of Slice Flip Flops	239	9312	2%
Number of 4 input LUTs	8174	9312	87%
Number of bonded IOBs	3	232	1%
Number of MULT 18X 18SIOs	16	20	80%
Number of GCLKs	2	24	8%

V. CONCLUSION

A OFDM modulator and demodulator were designed successfully where the power is major application and area also reduce, because design of FFT and I FFT in same block first we design FFT and the get output is right shift Three bits we can perform the IFFT function so one of the best real time application and also resource utilization is less compared to all the digital techniques. Compare throw previous technique SDR, it is only for higher and lower data transmission but OFDM use any of digital modulation techniques, and where the using only 1MHz clock for the entire project and controlled by clock distributor. Each block is tested using Xilinx ISE. The complete resource utilization is 3.5% of number of flip flops and 75% of the slices LUTs and combinational path delay is very less0.293ns and much speed is 100 bauds. It is much faster than Ethernet.

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BIOGRAPHIES

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